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EXAMINER

TRIMMINGS, JOHN P

ART UNIT

PAPER NUMBER

2133

DATE MAILED: 03/02/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/976,554

Applicant(s)

DORSEY, MICHAEL C.

Examiner

John P Trimmings

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 12 October 2001.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-37 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-37 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☒ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 11/12/2001 is/are: a) ☐ accepted or b) ☒ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____.
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____.

DETAILED ACTION

Claims 1-37 are presented for examination.

Information Disclosure Statement

The examiner has considered the applicant's Disclosure Statements of 3/27/2003.

Drawings

1. The drawings are objected to because:
 - a. FIG.2 LSSD and STEP CLKS are not referred to in the disclosure.
 - b. FIG.9 LSSD_CLKA, LSSD_CLKB, LBST_SCAN_CLKA and LBST_SDCAN_CLKB are not referred to in the disclosure.

A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Specification

2. The disclosure is objected to because of the following informalities:
 - a. Page 5 line 25 recites "synchronous random access memory ("SRAMs")".
The statement is a combination of two terms; "Static Random Access Memory, an SRAM", and "Synchronous Dynamic Random Access Memory, an SDRAM", the terms of which are generally accepted in the

- art. The examiner suspects that the applicant wishes to recite a "static random access memory", but would like the applicant to respond as to the device type specifically intended. Appropriate correction is required.
- b. The disclosure is objected to because of the following informalities: page 7 line 11 describes engine 110 being configured by a 66 bit signal composed of a 32 bit vector and 33 bit seed. The sum of 32 and 33 is not 66. Appropriate correction is required.
 - c. The disclosure is objected to because of the following informalities: page 9 line 24 recites, "(bits B₂₆ to B₀)", but the examiner believes that it should read, "(bits B₃₀ to B₀)". Appropriate correction is required.
 - d. The disclosure is objected to because of the following informalities: page 10 line 3 recites, "LBST_STEP_STEPE", but the examiner cannot find this reference in FIG.9. Appropriate correction is required.
 - e. The disclosure is objected to because of the following informalities: page 10 line 11 recites, "components 150", but the examiner cannot find this reference in the drawings. Appropriate correction is required.
 - f. The disclosure is objected to because of the following informalities: page 11 line 19 and 22, page 13 line 32 recite, "ASIC 100", but the examiner cannot find this reference in the drawings, and believes it should read "ASIC 150". Appropriate correction is required.
 - g. The disclosure is objected to because of the following informalities: page 12 line 32 recites, "initialized them to...", but the examiner believes it

should read "initialized to...". Appropriate correction is required.

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

3. Claims 7 and 31 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter, which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. The claims specify using a "paranoid check" for a purpose within a MBIST signature register. The same term is mentioned in the disclosure but the term was never defined. The examiner, being one with ordinary skill in the art, is unsure of what the applicant means when using this term.

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claims 7 and 31 rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Where applicant acts as his or her own lexicographer to specifically define a term of a claim contrary to its ordinary meaning, the written description must clearly redefine the claim term and set forth the uncommon

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definition so as to put one reasonably skilled in the art on notice that the applicant intended to so redefine that claim term. *Process Control Corp. v. HydReclaim Corp.*, 190 F.3d 1350, 1357, 52 USPQ2d 1029, 1033 (Fed. Cir. 1999). The term "paranoid check" in claims 7 and 28 is used by the claim to mean a test which the examiner is not familiar, while the accepted meaning is "to check again by another means." The term is indefinite because the specification does not clearly redefine the term.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 1, 6, 7, 13, 15, 18, 20 are rejected under 35 U.S.C. 102(b) as being anticipated by Motika et al., U.S. Patent No. 5982189.

As per Claims 1 and 13:

Motika et al. teaches A dual mode built-in self-test controller (FIG.2 and column 4 lines 5-7), comprising: a logic built-in self-test domain (FIG.2 34, 38), including: a logic built-in self-test engine/means capable of executing a logic built-in self-test (FIG.2 34); and a logic built-in self-test signature/storage means generated by an execution of the logic built-in self-test (column 3 lines 39-67 and column 4 lines 1-5); and

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a memory built-in self-test domain (FIG.2 32, 36), including: a memory built-in self-test engine/means capable of executing a memory built-in self-test (FIG.2 32).

As per Claims 6 and 15:

Motika et al. teaches the dual mode built-in self-test controller of claim 1 and 13, wherein the memory built-in self-test domain (FIG.2 32, 36) further comprises a memory built-in self-test signature/storage means generated by an execution of the memory built-in self-test (column 3 lines 39-63).

As per Claim 7:

The claim limits Claim 6 in that the signature includes paranoid check results. Since the examiner is unsure of the meaning of "paranoid check", and has rejected the term under 35 USC 112(1) and 112(2), it is assumed that the signature register of Claim 6 includes results of the kind already taught by Motika et al. (see column 3 lines 39-63).

As per Claim 18:

Motika et al. teaches an integrated circuit device (column 1 lines 5-8), comprising: a plurality of memory components (FIG.2 36); a logic core (FIG.2 38); a testing interface (FIG.2 60); and a dual mode built-in self-test controller (FIG.2 50) controlled through the testing interface, comprising: a logic built-in self-test domain (FIG.2 34, 38), including: a logic built-in self-test engine (FIG.2 34) capable of executing a logic built-in self-test on the logic core (column 3 lines 64-67 and column 4 lines 1-5); and a logic built-in self-test signature generated by an execution of the logic built-in self-test (column 3 lines 38-67 and column 4 lines 1-5); and a memory built-in self-test

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domain (FIG.2 32, 36), including: a memory built-in self-test engine (FIG.2 32) capable of executing a memory built-in self-test on the memory components (FIG.2 36).

As per Claim 20:

Motika et al. teaches the integrated circuit device of claim 18, wherein the memory built-in self-test domain (FIG.2 32, 36) further comprises a memory built-in self-test signature register generated by an execution of the memory built-in self-test (column 3 lines 41-63).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

The factual inquiries set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
 2. Ascertaining the differences between the prior art and the claims at issue.
 3. Resolving the level of ordinary skill in the pertinent art.
 4. Considering objective evidence present in the application indicating obviousness or nonobviousness.
6. Claims 2, 14 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Motika et al., U.S. Patent No. 5982189 as applied to Claim 1, 13 and 18 above, and in view of Koproski et al., U.S. Patent No. 6671838. The claims are dependent on

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Claim 1, 13 or 18 above, and limit the LBIST to comprise an LBIST state machine and pattern generator. In an analogous art, Koproski et al., in column 3 lines 1-5 teaches a state machine for an LBIST device, and, in FIG.1, Koproski et al. teaches a pattern generator 4. And in column 1 lines 1-67 and column 2 lines 1-28, the reference states the advantage of using a special analysis system for creating weighted patterns for testing in an LBIST. One with ordinary skill in the art at the time of the invention, motivated by Koproski et al., would combine the references, and so the claims are rejected.

7. Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Motika et al., U.S. Patent No. 5982189, in view of Koproski et al., U.S. Patent No. 6671838 as applied to Claim 2, and further in view of Zuraski et al., U.S. Patent No. 6560740, Lo et al., U.S. Patent No. 5661732, and Wong et al., U.S. Patent No. 6636997. The LBIST state machine in Claim 2 is further limited to a reset state entered via an external signal. Zuraski et al. enters a state via an external reset signal (Zuraski et al, column 10 lines 31-36), but does not begin initializing the device with an LBIST run signal. In an analogous art, Lo et al., enters a 1st state subsequent to a start ABIST signal (Lo et al. column 5 lines 6-8), and suggests a similar LBIST on the same chip (column 6 lines 9-12). And finally, Wong et al. in column 6 lines 26-50 teaches the states of scan, step, and complete (done) as specified by the applicant's claim. Wong et al., in column 2 lines 62-67, describes an advantage of the invention as being capable of both pseudo-random and functional testing. Lo et al. column 2 lines 38-40 lists an advantage of the invention as being an improvement in test time and test coverage. And Zuraski Jr. et al.,

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professes the advantages (column 2 lines 10-18) of a readily programmable BIST that would not need constant revision as needs change. In view of the motivations for Zuraski et al. and Lo et al., and in view of Wong et al., one with ordinary skill in the art at the time of the invention, would combine all of the references above, thus the claim is rejected.

8. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Motika et al., U.S. Patent No. 5982189, in view of Koproski et al., U.S. Patent No. 6671838 as applied to Claim 2, and further in view of Rajski et al., U.S. Patent No. 6684358. The controller of Claim 2 is limited wherein the pattern generator is an LFSR seeded with a primitive polynomial. In an analogous art, Rajski et al., in column 8 lines 6-9 teaches such pattern generator. In column 2 lines 15-33, the Rajski et al. recites an improved pattern generator that allows fuller test coverage than predecessors. And one with ordinary skill in the art at the time of the invention, motivated as suggested by Rajski et al., would combine the references, and so the claim is rejected.

9. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Motika et al., U.S. Patent No. 5982189, in view of Koproski et al., U.S. Patent No. 6671838 as applied to Claim 2, in view of Hong-Shin Jun, U.S. Patent No. 6658611, and further in view of Au et al., U.S. Patent No. 6681359. The controller of Claim 2 is limited wherein the signature includes an error bit (Jun column 5 lines 43-63) and a "done" bit (Au et al. column 9 lines 25-33). Jun cites an improved programmable BIST using optimum test patterns (column 2 lines 10-13), and Au et al. cites control of BIST using a standard interface (column 2 lines 18-26). And one with ordinary skill in the art at the time of the

invention, motivated as suggested above, would combine the references, and therefore the claim is rejected.

10. Claims 8 and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Motika et al., U.S. Patent No. 5982189 as applied to Claim 6 and 18 above, in view of Au et al., U.S. Patent No. 6681359.

As per Claim 8:

In a similar art, Au et al. teaches the signature register as containing a test done bit in column 9 lines 25-33, and based on the motivation for Au et al. stated elsewhere, the claim is rejected.

As per Claim 24:

The integrated circuit device of claim 18 is limited wherein testing interface comprises a Joint Test Action Group tap controller. Au et al., in the Abstract teaches this feature, and in view of the motivation stated elsewhere, the claim is rejected.

11. Claims 9, 11 and 16, 17, 21 and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Motika et al., U.S. Patent No. 5982189, and in view of Zuraski Jr. et al., U.S. Patent No. 6560740. Dependent on Claim 1 or 13 or 18, Claims 9 or 21 limit the MBIST engine to comprise a MBIST state machine and Claim 11 or 17 or 22 limit to a plurality of state machines, whereas Claims 16 and 17 are based on a means, and a nested MBIST engine driving a state machine. In an analogous art, Zuraski Jr. et al. teaches the same hierarchy where an MBIST state machine(s) (FIG.1 20a, 20b) is/are driven by an MBIST engine (FIG.1 18) as is described in column 5 lines 40-54. And Zuraski Jr. et al., professes the advantages (column 2 lines 10-18) of a readily

programmable BIST that would not need constant revision as needs change. One with ordinary skill in the art at the time of the invention, motivated as suggested by Zuraski Jr. et al., would combine the references, and so the claims are rejected.

12. Claims 10 and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Motika et al., U.S. Patent No. 5982189, and in view of Zuraski Jr. et al., U.S. Patent No. 6560740 as applied to Claim 9 and 11 above, and further in view of Lo et al., U.S. Patent No. 5661732. The claims further limit the controller wherein the state machine comprises a reset state entered upon an external reset signal (Zuraski et al, column 10 lines 31-36). However Zuraski et al. does not further limit the machine to flushing and testing. In an analogous art, Lo et al., upon entering a 1st state subsequent to a start ABIST signal (Lo et al. column 5 lines 6-8), the next state produces internal resets of registers, and then as a programmable option, a flush of the memory may occur (column 13 lines 6-10) and then subsequent testing (same reference) may take place. At the end of the test, a state described by column 5 lines 17-35 occurs with the initiation of a test done signal (FIG.1 26). In Lo et al. column 2 lines 38-40 lists an advantage of the invention as being an improvement in test time and test coverage. One with ordinary skill in the art at the time of the invention, motivated by Lo et al., would combine the references, and so the claims are rejected.

13. Claim 23 is rejected under 35 U.S.C. 103(a) as being unpatentable over Motika et al., U.S. Patent No. 5982189, and in view of Kim et al., U.S. Patent No. 6148426. The integrated circuit device of claim 18 is limited wherein the memory components include a static random access memory device. In an analogous art, Kim et al. performs MBIST

operations on an SRAM (see Title). And as Kim et al. in column 1 lines 43-45 states as an advantage to be a smaller address generator, one with ordinary skill in the art at the time of the invention, motivated by Kim et al., would combine the references, and thus the claim is rejected.

14. Claims 25, 26, and 31 are rejected under 35 U.S.C. 103(a) as being unpatentable over Motika et al., U.S. Patent No. 5982189, and in view of Kraus et al., U.S. Patent No. 6587979.

As per Claim 25:

Motika et al. teaches a method for performing a BIST using a dual-mode controller (FIG.2 50), but does not specify that the controller be reset externally. However, in an analogous art, the MBIST of Kraus et al., resets the MBIST controller of FIG.7 by way of the tester 21 (column 9 lines 52-58), and performs an MBIST (column 15 lines 24-35), and obtaining results (column 8 lines 10-36) of the MBIST. Column 2 lines 32-40 of Kraus et al. explains the attributes of the invention as being a highly adaptable and flexible platform for testing memories, and one with ordinary skill in the art at the time of the invention, motivated by Kraus et al., would combine the references, as so the claim is rejected.

As per Claim 26:

Dependent on Claim 25, the claim limits the reset of the controller includes resetting the MBIST engine. Kraus et al., shows the path of the reset signal from the JTAG bus to the core wrapper (FIG.6) pattern generator, which is part of the MBIST

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engine. And in view of the motivation previously stated for Kraus et al., the claim is rejected.

As per Claim 31:

The claim limits Claim 25 in that a signature register includes paranoid check results. Since the examiner is unsure of the meaning of "paranoid check", and has rejected the term under 35 USC 112(1) and 112(2), it is assumed that the signature register of Motika et al. includes results of the kind already taught (see column 3 lines 39-63).

15. Claim 27 is rejected under 35 U.S.C. 103(a) as being unpatentable over Motika et al., U.S. Patent No. 5982189, and in view of Kraus et al., U.S. Patent No. 6587979 as applied to Claim 25, and further in view of Rajski et al., U.S. Patent No. 6684358.

Dependent on Claim 25, the claim limits resetting a MISR and a pattern generator in an LBIST. Rajski et al. performs these functions on an LBIST (column 4 lines 10-57), and in view of the motivation for Rajski et al. previously stated, the claim is rejected.

16. Claims 28 and 30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Motika et al., U.S. Patent No. 5982189, and in view of Kraus et al., U.S. Patent No. 6587979 as applied to Claim 25, and further in view of Zuraski et al., U.S. Patent No. 6560740, Lo et al., U.S. Patent No. 5661732, and Wong et al., U.S. Patent No. 6636997.

As per Claim 28:

The BIST state machine in Claim 25 is further limited to a reset state entered via an external signal. Zuraski et al. enters a state via an external reset signal (Zuraski et al,

column 10 lines 31-36), but does not begin initializing the device with an LBIST run signal. In an analogous art, Lo et al., enters a 1st state subsequent to a start ABIST signal (Lo et al. column 5 lines 6-8), and suggests a similar LBIST on the same chip (column 6 lines 9-12). And finally, Wong et al. in column 6 lines 26-50 teaches the states of scan, step, and complete (done) as specified by the applicant's claim. Wong et al., in column 2 lines 62-67, describes an advantage of the invention as being capable of both pseudo-random and functional testing. Lo et al. column 2 lines 38-40 lists an advantage of the invention as being an improvement in test time and test coverage. And Zuraski Jr. et al., professes the advantages (column 2 lines 10-18) of a readily programmable BIST that would not need constant revision as needs change. In view of the motivations for Zuraski et al. and Lo et al., and in view of Wong et al., one with ordinary skill in the art at the time of the invention, would combine all of the references above, thus the claim is rejected.

As per Claim 30:

The claim further limits the method wherein the state machine comprises a reset state entered upon an external reset signal (Zuraski et al, column 10 lines 31-36). However Zuraski et al. does not further limit the method to flushing and testing. In an analogous art, Lo et al., upon entering a 1st state subsequent to a start ABIST signal (Lo et al. column 5 lines 6-8), the next state produces internal resets of registers, and then as a programmable option, a flush of the memory may occur (column 13 lines 6-10) and then subsequent testing (same reference) may take place. At the end of the test, a state described by column 5 lines 17-35 occurs with the initiation of a test done signal (FIG.1

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26). In Lo et al. column 2 lines 38-40 lists an advantage of the invention as being an improvement in test time and test coverage. One with ordinary skill in the art at the time of the invention, motivated by Lo et al., would combine the references, and so the claim is rejected.

17. Claim 29 is rejected under 35 U.S.C. 103(a) as being unpatentable over Motika et al., U.S. Patent No. 5982189, and in view of Kraus et al., U.S. Patent No. 6587979 as applied to Claim 25,, and further in view of Zuraski et al., U.S. Patent No. 6560740, Lo et al., U.S. Patent No. 5661732, and Wong et al., U.S. Patent No. 6636997 as applied to Claim 28, in view of Hong-Shin Jun, U.S. Patent No. 6658611, and further in view of Au et al., U.S. Patent No. 6681359. The method of Claim 28 is limited wherein the signature (MISR) includes an error bit (Jun column 5 lines 43-63) and a "done" bit (Au et al. column 9 lines 25-33). Jun cites an improved programmable BIST using optimum test patterns (column 2 lines 10-13), and one with ordinary skill in the art at the time of the invention, motivated as suggested above and previously for Au et al., would combine the references, and therefore the claim is rejected.

18. Claim 32, 36 and 37 are rejected under 35 U.S.C. 103(a) as being unpatentable over Au et al., U.S. Patent No. 6681359, in view of Zuraski et al., U.S. Patent No. 6560740, and in view of Motika et al., U.S. Patent No. 5982189.

As per Claim 32:

Au et al. teaches a method for testing an integrated circuit device (see Abstract), the method comprising: interfacing the integrated circuit device with a tester (column 7 lines 31-34 and column 8 lines 29-31); and Zuraski et al. enters a state via an external

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reset signal (Zuraski et al, column 10 lines 31-36), performing a logic built-in self-test (Motika et al. column 3 lines 64-66), performing a memory built-in self-test (Motika et al. column 3 lines 39-43), and obtaining the results of the LBIST and MBIST (Motika et al. column 3 lines 55-60 and column 4 lines 1-3). And in view of the motivations previously stated for the references, the claim is rejected.

As per Claim 36:

Au et al. teaches the method of claim 32, and obtaining the results by reading the signature (column 10 lines 21-26). And in view of the previously stated motivation, the claim is rejected.

As per Claim 37:

Au et al. teaches the method of claim 32, wherein interfacing the integrated circuit device with the tester includes employing Joint Test Action Group protocols (column 10 lines 21-25). And in view of the previously stated motivation, the claim is rejected.

19. Claim 33 is rejected under 35 U.S.C. 103(a) as being unpatentable over Au et al., U.S. Patent No. 6681359, in view of Zuraski et al., U.S. Patent No. 6560740, and in view of Motika et al., U.S. Patent No. 5982189 as applied to Claim 32 above, and further in view of Kraus et al., U.S. Patent No. 6587979. Motika et al. teaches a method for performing a BIST using a dual-mode controller (FIG.2 50), but does not specify that the controller be reset. However, in an analogous art, the MBIST of Kraus et al., resets the MBIST controller of FIG.7 by way of the tester 21 (column 9 lines 52-58), and in view of the motivation previously stated, the claim is rejected.

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20. Claim 34 is rejected under 35 U.S.C. 103(a) as being unpatentable over Au et al., U.S. Patent No. 6681359, in view of Zuraski et al., U.S. Patent No. 6560740, and in view of Motika et al., U.S. Patent No. 5982189 as applied to Claim 32 above, and further in view of Lo et al., U.S. Patent No. 5661732, and Wong et al., U.S. Patent No. 6636997. In an analogous art, Lo et al., enters a 1st state subsequent to a start ABIST signal (Lo et al. column 5 lines 6-8), and suggests a similar LBIST on the same chip (column 6 lines 9-12). And finally, Wong et al. in column 6 lines 26-50 teaches the states of scan, step, and complete (done) as specified by the applicant's claim. Wong et al., in column 2 lines 62-67, describes an advantage of the invention as being capable of both pseudo-random and functional testing. In view of the elsewhere stated motivations for Lo et al., and of Wong et al., one with ordinary skill in the art at the time of the invention, would combine all of the references above, thus the claim is rejected.

21. Claim 35 is rejected under 35 U.S.C. 103(a) as being unpatentable over Au et al., U.S. Patent No. 6681359, in view of Zuraski et al., U.S. Patent No. 6560740, and in view of Motika et al., U.S. Patent No. 5982189 as applied to Claim 32 above, and further in view of Lo et al., U.S. Patent No. 5661732. In an analogous art, Lo et al., upon enters a 1st state subsequent to a start ABIST signal (Lo et al. column 5 lines 6-8), the next state producing internal resets of registers, and then as a programmable option, a flush of the memory may occur (column 13 lines 6-10) and then subsequent testing (same reference) may take place. At the end of the test, a state described by column 5 lines 17-35 occurs with the initiation of a test done signal (FIG.1 26). In Lo et al. column 2 lines 38-40 lists an advantage of the invention as being an improvement in test time

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and test coverage. One with ordinary skill in the art at the time of the invention, motivated by Lo et al., would combine the references, and so the claim is rejected. storing the indication (column 9 lines 25-34); and reading the indication (column 10 lines 21-26).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to John P Trimmings whose telephone number is 703-305-0714. The examiner can normally be reached on weekdays, 7:30 AM to 4:00 PM.

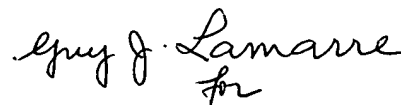
If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert DeCady can be reached on 703-305-9595. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

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John P Trimmings
Examiner
Art Unit 2133

jpt



Albert DeCady
Primary Examiner

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